3
Hardware Interface

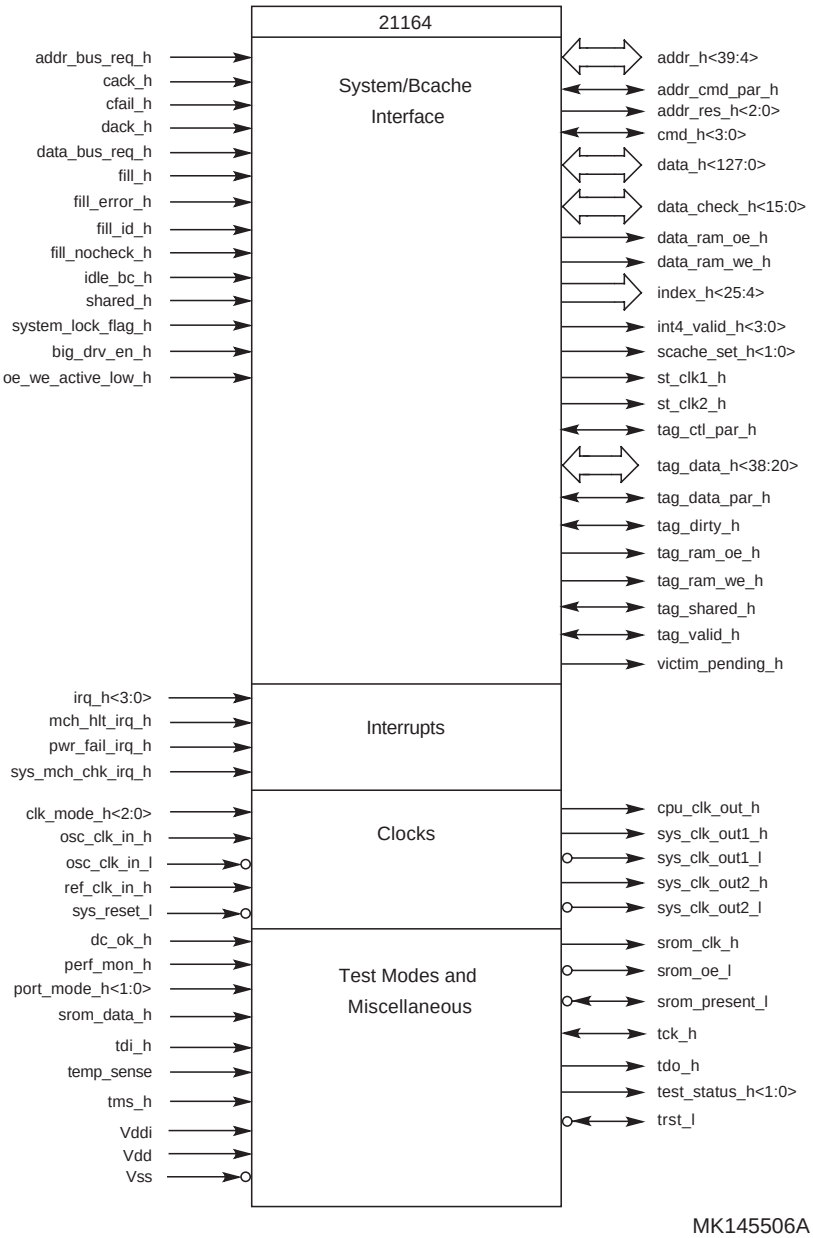
This chapter contains the 21164 microprocessor logic symbol and provides a list of signal names and their functions.

3.1 21164 Microprocessor Logic Symbol

Figure 3–1 shows the logic symbol for the 21164 chip.

21164 Microprocessor Logic Symbol

Figure 3–1 21164 Microprocessor Logic Symbol



3.2 21164 Signal Names and Functions

The 21164 is contained in a 499-pin interstitial pin grid array (IPGA) package. There are 296 functional signal pins, 3 spare (unused) signal pins, 39 external power (**Vdd**) pins, 65 internal power (**Vddi**) pins, and 96 ground (**Vss**) pins.

The following table defines the 21164 signal types referred to in this section:

Signal Type	Definition
B	Bidirectional
I	Input only
O	Output only

The remaining two tables describe the function of each 21164 external signal. Table 3–1 lists all signals in alphanumeric order. This table provides full signal descriptions. Table 3–2 lists signals by function and provides an abbreviated description.

21164 Signal Names and Functions

Table 3–1 21164 Signal Descriptions *(Sheet 1 of 12)*

Signal	Type	Count	Description
addr_h<39:4>	B	36	Address bus. These bidirectional signals provide the address of the requested data or operation between the 21164 and the system. If **addr_h<39>** is asserted, then the reference is to non-cached, I/O memory space. When the byte/word instructions are enabled and **addr_h<39>** is asserted, 6 additional bits of information are communicated over the pin bus. Two of the new bits are driven over **addr_h<38:37>**, becoming **transfer_size<1:0>**, with the following values: 00 Size = 8 bytes 01 Size = 4 bytes 10 Size = 2 bytes 11 Size = 1 byte
addr_bus_req_h	I	1	Address bus request. The system interface uses this signal to gain control of the **addr_h<39:4>**, **addr_cmd_par_h**, and **cmd_h<3:0>** pins (see Figure 4–32).
addr_cmd_par_h	B	1	Address command parity. This is the odd parity bit on the current command and address buses. The 21164 takes a machine check if a parity error is detected. The system should do the same if it detects an error.
addr_res_h<1:0>	O	2	Address response bits <1> and <0>. For system commands, the 21164 uses these pins to indicate the state of the block in the Scache:

Bits	Command	Meaning
00	NOP	Nothing.
01	NOACK	Data not found or clean.
10	ACK/Scache	Data from Scache.
11	ACK/Bcache	Data from Bcache.

Table 3–1 21164 Signal Descriptions *(Sheet 2 of 12)*

Signal	Type	Count	Description
addr_res_h<2>	O	1	Address response bit <2>. For system commands, the 21164 uses this pin to indicate if the command hits in the Scache or onchip load lock register.
big_drv_en_h	I	1	This signal provides the ability to change the output drive characteristics of **index<25:4>, st_clk1_h, st_clk2_h, data_ram_oe_h, data_ram_we_h, tag_ram_oe_h,** and **tag_ram_we_h**. When asserted, **big_drv_en_h** increases the drive capability of these signals by 50%, eliminating the need to buffer these heavily loaded signals. This signal is defined during power-up and *must* not change state during operation.
cack_h	I	1	Command acknowledge. The system interface uses this signal to acknowledge any one of the commands driven by the 21164.
cfail_h	I	1	Command fail. This signal has two uses. It can be asserted during a cack cycle of a WRITE BLOCK LOCK command to indicate that the write operation is not successful. In this case, both **cack_h** and **cfail_h** are asserted together. It can also be asserted instead of **cack_h** to force an instruction fetch/decode unit (IDU) timeout event. This causes the 21164 to do a partial reset and trap to the machine check (MCHK) PALcode entry point, which indicates a serious hardware error.

Table 3–1 21164 Signal Descriptions *(Sheet 3 of 12)*

Signal	Type	Count	Description
clk_mode_h<2:0>	I	3	Clock test mode. These signals specify a relationship between **osc_clk_in_h**,**l** and the CPU cycle time. These signals should be deasserted in normal operation mode.

Bits	Divisor	Description
000	2	CPUclock frequency is one-half of input clock frequency.
001	1	CPUclock frequency is equal to the input clock frequency, but the onchip duty-cycle equalizer is disabled.
010	4	CPU clock frequency is one-fourth of input clock frequency.
011	—	Initialize the CPU clock, allowing the system clock to be synchronized to a stable reference clock.
101	1	CPU clock frequency is equal to input clock frequency, and the onchip duty-cycle equalizer is enabled. **This is the preferred mode for normal operation**.
100/11x	—	Not valid configurations.

Table 3–1 21164 Signal Descriptions *(Sheet 4 of 12)*

Signal	Type	Count	Description
cmd_h<3:0>	B	4	Command bus. These signals drive and receive the commands from the command bus. The following tables define the commands that can be driven on the **cmd_h<3:0>** bus by the 21164 or the system. For additional information, refer to Section 4.1.1.1.

21164 Commands to System:

cmd_h <3:0>	Command	Meaning
0000	NOP	Nothing.
0001	LOCK	Lock register address.
0010	FETCH	The 21164 passes a FETCH instruction to the system.
0011	FETCH_M	The 21164 passes a FETCH_M instruction to the system.
0100	MEMORY BARRIER	MB instruction.
0101	SET DIRTY	Dirty bit set if shared bit is clear.
0110	WRITE BLOCK	Request to write a block.
0111	WRITE BLOCK LOCK	Request to write a block with lock.
1000	READ MISS0	Request for data.
1001	READ MISS1	Request for data.
1010	READ MISS MOD 0	Request for data; modify intent.
1011	READ MISS MOD 1	Request for data; modify intent.
1100	BCACHE VICTIM	Bcache victim should be removed.

Table 3–1 21164 Signal Descriptions *(Sheet 5 of 12)*

Signal	Type	Count	Description

1101	—	Reserved
1110	READ MISS STC0	Request for data; ST*x*_C data.
1111	READ MISS STC1	Request for data; ST*x*_C data.

System Commands to 21164:

cmd_h <3:0>	Command	Meaning
0000	NOP	Nothing.
0001	FLUSH	Removes block from caches; return dirty data.
0010	INVALIDATE	Invalidates the block from caches.
0011	SET SHARED	Block goes to the shared state.
0100	READ	Read a block.
0101	READ DIRTY	Read a block; set shared.
0111	READ DIRTY/INV	Read a block; invalidate.

cpu_clk_out_h	O	1	CPU clock output. This signal is used for test purposes.
dack_h	I	1	Data acknowledge. The system interface uses this signal to control data transfer between the 21164 and the system.
data_h<127:0>	B	128	Data bus. These signals are used to move data between the 21164, the system, and the Bcache.
data_bus_req_h	I	1	Data bus request. If the 21164 samples this signal asserted on the rising edge of sysclk *n*, then the 21164 does not drive the data bus on the rising edge of sysclk *n*+1. Before asserting this signal, the system should assert **idle_bc_h** for the correct number of cycles. If the 21164 samples this signal deasserted on the rising edge of sysclk *n*, then the 21164 drives the data bus on the rising edge of sysclk *n*+1. For timing details, refer to Section 4.11.4.

Table 3–1 21164 Signal Descriptions *(Sheet 6 of 12)*

Signal	Type	Count	Description
data_check_h<15:0>	B	16	Data check. These signals set even byte parity or INT8 ECC for the current data cycle. Refer to Section 4.14.1 for information on the purpose of each **data_check_h** bit.
data_ram_oe_h	O	1	Data RAM output enable. This signal is asserted for Bcache read operations.
data_ram_we_h	O	1	Data RAM write-enable. This signal is asserted for any Bcache write operation. Refer to Section 5.3.5 for timing details.
dc_ok_h	I	1	dc voltage OK. Must be deasserted until dc voltage reaches proper operating level. After that, **dc_ok_h** is asserted.
fill_h	I	1	Fill warning. If the 21164 samples this signal asserted on the rising edge of sysclk *n*, then the 21164 provides the address indicated by **fill_id_h** to the Bcache on the rising edge of sysclk *n*+1. The Bcache begins to write in that sysclk. At the end of sysclk *n*+1, the 21164 waits for the next sysclk and then begins the write operation again if **dack_h** is not asserted. Refer to Section 4.11.3 for timing details.
fill_error_h	I	1	Fill error. If this signal is asserted during a fill from memory, it indicates to the 21164 that the system has detected an invalid address or hard error. The system still provides an apparently normal read sequence with correct ECC/parity though the data is not valid. The 21164 traps to the machine check (MCHK) PALcode entry point and indicates a serious hardware error. **fill_error_h** should be asserted when the data is returned. Each assertion produces a MCHK trap.
fill_id_h	I	1	Fill identification. Asserted with **fill_h** to indicate which register is used. The 21164 supports two outstanding load instructions. If this signal is asserted when the 21164 samples **fill_h** asserted, then the 21164 provides the address from miss register 1. If it is deasserted, then the address in miss register 0 is used for the read operation.
fill_nocheck_h	I	1	Fill checking off. If this signal is asserted, then the 21164 does not check the parity or ECC for the current data cycle on a fill.
idle_bc_h	I	1	Idle Bcache. When asserted, the 21164 finishes the current Bcache read or write operation but does not start a new read or write operation until the signal is deasserted. The system interface must assert this signal in time to idle the Bcache before fill data arrives.

Table 3–1 21164 Signal Descriptions *(Sheet 7 of 12)*

Signal	Type	Count	Description
index_h<25:4>	O	22	Index. These signals index the Bcache.
int4_valid_h<3:0>	O	4	INT4 data valid. During write operations to noncached space, these signals are used to indicate which INT4 bytes of data are valid. This is useful for noncached write operations that have been merged in the write buffer.

int4_valid_h<3:0>	Write Meaning
xxx1	**data_h<31:0>** valid
xx1x	**data_h<63:32>** valid
x1xx	**data_h<95:64>** valid
1xxx	**data_h<127:96>** valid

During read operations to noncached space, these signals indicate which INT8 bytes of a 32-byte block need to be read and returned to the processor. This is useful for read operations to noncached memory.

int4_valid_h<3:0>	Read Meaning
xxx1	**data_h<63:0>** valid
xx1x	**data_h<127:64>** valid
x1xx	**data_h<191:128>** valid
1xxx	**data_h<255:192>** valid

Note: For both read and write operations, multiple **int4_valid_h<3:0>** bits can be set simultaneously.

When **addr_h<39>** is asserted, the **int4_valid_h<3:0>** signals are considered the **addr_h<3:0>** bits required for byte/word transactions. The functionality of these bits is tied to the value stored in **addr_h<38:37>**.

Table 3–1 21164 Signal Descriptions *(Sheet 8 of 12)*

Signal	Type	Count	Description
			For Read Transactions:

addr_h <38:37>	int4_valid_h<3:0> Value
00	Valid INT8 mask
01	**addr_h<3:2>** valid on **int4_valid_h<3:2>**; **int4_valid<1:0>** undefined
10	**addr_h<3:1>** valid on **int4_valid_h<3:1>**; **int4_valid<0>** undefined
11	**addr_h<3:0>** valid on **int4_valid_h<3:0>**

For Write Transactions:

addr_h <38:37>	int4_valid_h<3:0> Value
00	Valid INT4 mask
01	Valid INT4 mask
10	**addr_h<3:1>** valid on **int4_valid_h<3:1>**; **int4_valid<0>** undefined
11	**addr_h<3:0>** valid on **int4_valid_h<3:0>**

Table 3–1 21164 Signal Descriptions *(Sheet 9 of 12)*

Signal	Type	Count	Description
irq_h<3:0>	I	4	System interrupt requests. These signals have multiple modes of operation. During normal operation, these level-sensitive signals are used to signal interrupt requests. During initialization, these signals are used to set up the CPU cycle time divisor for **sys_clk_out1_h,l** as follows:

irq_h<3>	irq_h<2>	irq_h<1>	irq_h<0>	Ratio
Low	Low	High	High	3
Low	High	Low	Low	4
Low	High	Low	High	5
Low	High	High	Low	6
Low	High	High	High	7
High	Low	Low	Low	8
High	Low	Low	High	9
High	Low	High	Low	10
High	Low	High	High	11
High	High	Low	Low	12
High	High	Low	High	13
High	High	High	Low	14
High	High	High	High	15

mch_hlt_irq_h	I	1	Machine halt interrupt request. This signal has multiple modes of operation. During initialization, this signal is used to set up **sys_clk_out2_ h,l** delay (see Table 4–3). During normal operation, it is used to signal a halt request.
oe_we_active_low_h	I	1	This signal provides the ability to control the polarity of the offchip cache RAM control signals (**data_ram_ oe_h, data_ram_we_h, tag_ram_oe_h,** and **tag_ram_we_h**). When this signal is deasserted, the offchip cache signals are asserted high. When this signal is asserted, the assertion levels of the cache signals are inverted to a low level. This signal is defined during power-up and must not change state during operation.

Table 3–1 21164 Signal Descriptions *(Sheet 10 of 12)*

Signal	Type	Count	Description
osc_clk_in_h **osc_clk_in_l**	I I	1 1	Oscillator clock inputs. These signals provide the differential clock input that is the fundamental timing of the 21164. These signals are driven at the same frequency as the internal clock frequency (**clk_mode_h<2:0>** = 101).
perf_mon_h	I	1	Performance monitor. This signal can be used as an input to the 21164 internal performance monitoring hardware from offchip events (such as bus activity). Refer to Section 5.1.27 for information on the PMCTR register.
port_mode_h<1:0>	I	2	Select test port interface modes (normal, manufacturing, and debug). For normal operation, both signals must be deasserted.
pwr_fail_irq_h	I	1	Power failure interrupt request. This signal has multiple modes of operation. During initialization, this signal is used to set up **sys_clk_out2_ h,l** delay (see Table 4–3). During normal operation, this signal is used to signal a power failure.
ref_clk_in_h	I	1	Reference clock input. Optional. Used to synchronize the timing of multiple microprocessors to a single reference clock. If this signal is not used, it must be tied to **Vdd** for proper operation.
scache_set_h<1:0>	O	2	Secondary cache set. During a read miss request, these signals indicate the Scache set number that will be filled when the data is returned. This information can be used by the system to maintain a duplicate copy of the Scache tag store.
shared_h	I	1	Keep block status shared. For systems without a Bcache, when a WRITE BLOCK/NO VICTIM PENDING or WRITE BLOCK LOCK command is acknowledged, this pin can be used to keep the block status shared or private in the Scache.
srom_clk_h	O	1	Serial ROM clock. Supplies the clock that causes the SROM to advance to the next bit. The cycle time of this clock is 128 times the cycle time of the CPU clock.
srom_data_h	I	1	Serial ROM data. Input for the SROM.
srom_oe_l	O	1	Serial ROM output enable. Supplies the output enable to the SROM.
srom_present_l[1]	B	1	Serial ROM present. Indicates that SROM is present and ready to load the Icache.

Table 3–1 21164 Signal Descriptions *(Sheet 11 of 12)*

Signal	Type	Count	Description
st_clk1_h	O	1	STRAM clock. Clock for synchronously timed RAMs (STRAMs). For Bcache, this signal is synchronous with **index_h<25:4>** during private read and write operations, and with **sys_clk_out1_h,l** during read and fill operations. BC_CONTROL<26> must be set to use this.
st_clk2_h	O	1	This signal is a duplicate of **st_clk1_h**, increasing the fanout capability of the signal.
sys_clk_out1_h **sys_clk_out1_l**	O O	1 1	System clock outputs. Programmable system clock (**cpu_clk_out_h** divided by a value of 3 to 15) is used for board-level cache and system logic.
sys_clk_out2_h **sys_clk_out2_l**	O O	1 1	System clock outputs. A version of **sys_clk_out1_h,l** delayed by a programmable amount from 0 to 7 CPU cycles.
sys_mch_chk_irq_h	I	1	System machine check interrupt request. This signal has multiple modes of operation. During initialization, it is used to set up **sys_clk_out2_h,l** delay (see Table 4–3). During normal operation, it is used to signal a machine interrupt check request.
sys_reset_l	I	1	System reset. This signal protects the 21164 from damage during initial power-up. It must be asserted until **dc_ok_h** is asserted. After that, it is deasserted and the 21164 begins its reset sequence.
system_lock_flag_h	I	1	System lock flag. During fills, the 21164 logically ANDs the value of the system copy with its own copy to produce the true value of the lock flag.
tag_ctl_par_h	B	1	Tag control parity. This signal indicates odd parity for **tag_valid_h, tag_shared_h,** and **tag_dirty_h**. During fills, the system should drive the correct parity based on the state of the valid, shared, and dirty bits.
tag_data_h<38:20>	B	19	Bcache tag data bits. This bit range supports 1MB to 64MB Bcaches.
tag_data_par_h	B	1	Tag data parity bit. This signal indicates odd parity for **tag_data_h<38:20>**.
tag_dirty_h	B	1	Tag dirty state bit. During fills, the system should assert this signal if the 21164 request is a READ MISS MOD, and the shared bit is not asserted. Refer to Table 4–6 for information about Bcache protocol.

Table 3–1 21164 Signal Descriptions *(Sheet 12 of 12)*

Signal	Type	Count	Description
tag_ram_oe_h	O	1	Tag RAM output enable. This signal is asserted during any Bcache read operation.
tag_ram_we_h	O	1	Tag RAM write-enable. This signal is asserted during any tag write operation. During the first CPU cycle of a write operation, the write pulse is deasserted. In the second and following CPU cycles of a write operation, the write pulse is asserted if the corresponding bit in the write pulse register is asserted. Bits BC_WE_CTL<8:0> control the shape of the pulse (see Section 5.3.5).
tag_shared_h	B	1	Tag shared bit. During fills, the system should drive this signal with the correct value to mark the cache block as shared. See Table 4–6 for information about Bcache protocol.
tag_valid_h	B	1	Tag valid bit. During fills, this signal is asserted to indicate that the block has valid data. See Table 4–6 for information about Bcache protocol.
tck_h	B	1	JTAG boundary-scan clock.
tdi_h	I	1	JTAG serial boundary-scan data-in signal.
tdo_h	O	1	JTAG serial boundary-scan data-out signal.
temp_sense	I	1	Temperature sense. This signal is used to measure the die temperature and is for manufacturing use only. For normal operation, this signal must be left disconnected.
test_status_h<1:0>	O	2	Icache test status. These signals are used for manufacturing test purposes only to extract Icache test status information from the chip. **test_status_h<0>** is asserted if ICSR<39> is true, on IDU timeout, or remains asserted if the Icache built-in self-test (BiSt) fails. Also, **test_status_h<0>** outputs the value written by PALcode to **test_status_h<1>** through IPR access. For additional information, refer to Section 12.2.2.
tms_h	I	1	JTAG test mode select signal.
trtst_l[1]	B	1	JTAG test access port (TAP) reset signal.
victim_pending_h	O	1	Victim pending. When asserted, this signal indicates that the current read miss has generated a victim.

[1]This signal is shown as bidirectional. However, for normal operation, it is input only. The output function is used during manufacturing test and verification only.

21164 Signal Names and Functions

Table 3–2 lists signals by function and provides an abbreviated description.

Table 3–2 21164 Signal Descriptions by Function *(Sheet 1 of 3)*

Signal	Type	Count	Description
Clocks			
clk_mode_h<2:0>	I	3	Clock test mode.
cpu_clk_out_h	O	1	CPU clock output.
osc_clk_in_h,l	I	2	Oscillator clock inputs.
ref_clk_in_h	I	1	Reference clock input.
st_clk1_h	O	1	Bcache STRAM clock output.
st_clk2_h	O	1	Bcache STRAM clock output.
sys_clk_out1_h,l	O	2	System clock outputs.
sys_clk_out2_h,l	O	2	System clock outputs.
sys_reset_l	I	1	System reset.
Bcache			
big_drv_en_h	I	1	Increase drive capability enable.
data_h<127:0>	B	128	Data bus.
data_check_h<15:0>	B	16	Data check.
data_ram_oe_h	O	1	Data RAM output enable.
data_ram_we_h	O	1	Data RAM write-enable.
index_h<25:4>	O	22	Index.
oe_we_active_low_h	I	1	Assertion-level control signal.
tag_ctl_par_h	B	1	Tag control parity.
tag_data_h<38:20>	B	19	Bcache tag data bits.
tag_data_par_h	B	1	Tag data parity bit.
tag_dirty_h	B	1	Tag dirty state bit.
tag_ram_oe_h	O	1	Tag RAM output enable.
tag_ram_we_h	O	1	Tag RAM write-enable.
tag_shared_h	B	1	Tag shared bit.

Table 3–2 21164 Signal Descriptions by Function *(Sheet 2 of 3)*

Signal	Type	Count	Description
tab_valid_h	B	1	Tag valid bit.
System Interface			
addr_h<39:4>	B	36	Address bus.
addr_bus_req_h	I	1	Address bus request.
addr_cmd_par_h	B	1	Address command parity.
addr_res_h<2:0>	O	3	Address response.
cack_h	I	1	Command acknowledge.
cfail_h	I	1	Command fail.
cmd_h<3:0>	B	4	Command bus.
dack_h	I	1	Data acknowledge.
data_bus_req_h	I	1	Data bus request.
fill_h	I	1	Fill warning.
fill_error_h	I	1	Fill error.
fill_id_h	I	1	Fill identification.
fill_nocheck_h	I	1	Fill checking off.
idle_bc_h	I	1	Idle Bcache.
int4_valid_h<3:0>	O	4	INT4 data valid.
scache_set_h<1:0>	O	2	Secondary cache set.
shared_h	I	1	Keep block status shared.
system_lock_flag_h	I	1	System lock flag.
victim_pending_h	O	1	Victim pending.
Interrupts			
irq_h<3:0>	I	4	System interrupt requests.
mch_hlt_irq_h	I	1	Machine halt interrupt request.
pwr_fail_irq_h	I	1	Power fail interrupt request.

21164 Signal Names and Functions

Table 3–2 21164 Signal Descriptions by Function *(Sheet 3 of 3)*

Signal	Type	Count	Description
sys_mch_chk_irq_h	I	1	System machine check interrupt request.
Test Modes and Miscellaneous			
dc_ok_h	I	1	dc voltage OK.
perf_mon_h	I	1	Performance monitor.
port_mode_h<1:0>	I	2	Select test port interface mode (normal, manufacturing, and debug).
srom_clk_h	O	1	Serial ROM clock.
srom_data_h	I	1	Serial ROM data.
srom_oe_l	O	1	Serial ROM output enable.
srom_present_l[1]	B	1	Serial ROM present.
tck_h	B	1	JTAG boundary-scan clock.
tdi_h	I	1	JTAG serial boundary-scan data in.
tdo_h	O	1	JTAG serial boundary-scan data out.
temp_sense	I	1	Temperature sense.
test_status_h<1:0>	O	2	Icache test status.
tms_h	I	1	JTAG test mode select.
trst_l[1]	B	1	JTAG test access port (TAP) reset.

[1]This signal is shown as bidirectional. However, for normal operation, it is input only. The output function is used during manufacturing test and verification only.