

## 8 Internal Processor Registers

The tables in this section provide a summary of the 21164 implementation-specific internal processor registers (IPRs). For detailed register information, see the *Samsung 21164 Alpha Microprocessor Hardware Reference Manual*. For more information about the architecturally specified IPRs, see the *Alpha AXP Architecture Reference Manual*.

### 8.1 IDU, MTU, Dcache, and PALtemp IPRs

Table 10 lists the IDU, MTU, data cache (Dcache), and PALtemp IPRs. These IPRs are accessible to PALcode by means of the HW\_MTPR and HW\_MFPR instructions, using the IPR index. The IDU holds a bank of 24 PALtemp registers.

**table 10 IDU, MTU, Dcache, and PALtemp IPRs** (Sheet 1 of 4)

IPR Mnemonic	Register Name	Access	Index <sub>16</sub>
<b>IDU IPRs</b>			
ISR	Interrupt Summary	R	100
ITB_TAG	Istream translation buffer tag	W	101
ITB_PTE	Instruction translation buffer page table entry	R/W	102
ITB_ASN	Instruction translation buffer address space number	R/W	103
ITB_PTE_TEMP	Instruction translation buffer page table entry temporary	R	104
ITB_IA	Instruction translation buffer invalidate all	W	105
ITB_IAP	Instruction translation buffer invalidate all process	W	106
ITB_IS	Instruction translation buffer invalidate single	W	107
SIRR	Software interrupt request	R/W	108
ASTRR	Asynchronous system trap request	R/W	109
ASTER	Asynchronous system trap enable	R/W	10A
EXC_ADDR	Exception address	R/W	10B

## IDU, MTU, Dcache, and PALtemp IPRs

**table 10 IDU, MTU, Dcache, and PALtemp IPRs**

(Sheet 2 of 4)

IPR Mnemonic	Register Name	Access	Index <sub>16</sub>
EXC_SUM	Exception summary	R/W0C	10C
EXC_MASK	Exception mask	R	10D
PAL_BASE	Privileged architecture library base address	R/W	10E
ICM	IDU current mode	R/W	10F
IPLR	Interrupt priority level	R/W	110
INTID	Interrupt ID	R	111
IFAULT_VA_FORM	Formatted faulting virtual address	R	112
IVPTBR	Virtual page table base	R/W	113
HWINT_CLR	Hardware interrupt clear	W	115
SL_XMIT	Serial line transmit	W	116
SL_RCV	Serial line receive	R	117
ICSR	IDU control and status	R/W	118
IC_FLUSH_CTL	Icache flush control	W	119
ICPERR_STAT	Icache parity error status	R/W1C	11A
PMCTR	Performance counter	R/W	11C
<b>PALtemp IPRs</b>			
PALtemp0	—	R/W	140
PALtemp1	—	R/W	141
PALtemp2	—	R/W	142
PALtemp3	—	R/W	143
PALtemp4	—	R/W	144
PALtemp5	—	R/W	145
PALtemp6	—	R/W	146
PALtemp7	—	R/W	147
PALtemp8	—	R/W	148

## IDU, MTU, Dcache, and PALtemp IPRs

**table 10 IDU, MTU, Dcache, and PALtemp IPRs**

*(Sheet 3 of 4)*

IPR Mnemonic	Register Name	Access	Index <sub>16</sub>
PALtemp9	—	R/W	149
PALtemp10	—	R/W	14A
PALtemp11	—	R/W	14B
PALtemp12	—	R/W	14C
PALtemp13	—	R/W	14D
PALtemp14	—	R/W	14E
PALtemp15	—	R/W	14F
PALtemp16	—	R/W	150
PALtemp17	—	R/W	151
PALtemp18	—	R/W	152
PALtemp19	—	R/W	153
PALtemp20	—	R/W	154
PALtemp21	—	R/W	155
PALtemp22	—	R/W	156
PALtemp23	—	R/W	157

### MTU IPRs

DTB_ASN	Dstream translation buffer address space number	W	200
DTB_CM	Dstream translation buffer current mode	W	201
DTB_TAG	Dstream translation buffer tag	W	202
DTB_PTE	Dstream translation buffer page table entry	R/W	203
DTB_PTE_TEMP	Dstream translation buffer page table entry temporary	R	204
MM_STAT	Dstream memory-management fault status	R	205
VA	Faulting virtual address	R	206

## External Interface Control (CBU) IPRs

**table 10** IDU, MTU, Dcache, and PALtemp IPRs

(Sheet 4 of 4)

IPR Mnemonic	Register Name	Access	Index <sub>16</sub>
VA_FORM	Formatted virtual address	R	207
MVPTBR	MTU virtual page table base	W	208
DTB_IAP	Dstream translation buffer invalidate all process	W	209
DTB_IA	Dstream translation buffer invalidate all	W	20A
DTB_IS	Dstream translation buffer invalidate single	W	20B
ALT_MODE	Alternate mode	W	20C
CC	Cycle counter	W	20D
CC_CTL	Cycle counter control	W	20E
MCSR	MTU control	R/W	20F
DC_FLUSH	Dcache flush	W	210
DC_PERR_STAT	Dcache parity error status	R/W1C	212
DC_TEST_CTL	Dcache test tag control	R/W	213
DC_TEST_TAG	Dcache test tag	R/W	214
DC_TEST_TAG_TEMP	Dcache test tag temporary	R/W	215
DC_MODE	Dcache mode	R/W	216
MAF_MODE	Miss address file mode	R/W	217

## 8.2 External Interface Control (CBU) IPRs

Table 11 summarizes IPRs for controlling Scache, Bcache, system configuration, and logging error information. These IPRs cannot be read or written from the system. They are placed in the 1MB region of 21164-specific I/O address space ranging from FF FFF0 0000 to FF FFFF FFFF. Any read or write operation to an undefined IPR in this address space produces UNDEFINED behavior. The operating system should not map any address in this region as writable in any mode.

## PALcode Storage Registers

**table 11 CBU Internal Processor Register Descriptions**

Register	Description	Type <sup>1</sup>	Address
SC_CTL	Scache control	RW	FF FFF0 00A8
SC_STAT	Scache status	R	FF FFF0 00E8
SC_ADDR	Scache address	R	FF FFF0 0188
BC_CONTROL	Bcache control	W	FF FFF0 0128
BC_CONFIG	Bcache configuration	W	FF FFF0 01C8
BC_TAG_ADDR	Bcache tag address	R	FF FFF0 0108
EL_STAT	External interface status	R	FF FFF0 0168
EL_ADDR	External interface address	R	FF FFF0 0148
FILL_SYN	Fill syndrome	R	FF FFF0 0068

<sup>1</sup> BC\_CONTROL<01> must be 0 when reading any IPR in this table.

### 8.3 PALcode Storage Registers

The 21164 IEU register file has eight extra registers that are called the PALshadow registers. The PALshadow registers overlay R8 through R14 and R25 when the CPU is in PALmode and ICSR<SDE> is set. Thus, PALcode can consider R8 through R14 and R25 as local scratch. PALshadow registers cannot be written in the last two cycles of a PALcode flow. The normal state of the CPU is ICSR<SDE> = ON. PALcode disables SDE for the unaligned trap and for error flows.