

## PALcode Entry Points

# 9 PALcode

Privileged architecture library code (PALcode) is macrocode that provides an architecturally defined operating-system-specific programming interface that is common across all Alpha microprocessors. The actual implementation of PALcode differs for each operating system.

PALcode runs with privileges enabled, instruction stream (Istream) mapping disabled, and interrupts disabled. PALcode has privilege to use five special opcodes that allow functions such as physical data stream (Dstream) references and internal processor register (IPR) manipulation.

PALcode can be invoked by the following events:

- Reset
- System hardware exceptions (MCHK, ARITH)
- Memory-management exceptions
- Interrupts
- CALL\_PAL instructions

## 9.1 PALcode Entry Points

PALcode is invoked at specific entry points. The 21164 has two types of PALcode entry points:

- CALL\_PAL entry points are used whenever the IDU encounters a CALL\_PAL instruction in the Istream.
  - Privileged CALL\_PAL instructions start at offset  $2000_{16}$ .
  - Unprivileged CALL\_PAL instructions start at offset  $3000_{16}$ .
- Chip-specific trap entry points start PALcode.

## PALcode Entry Points

### 9.1.1 PALcode Trap Entry Points

Table 12 shows the PALcode trap entry points and their offset from the PAL\_BASE IPR. Entry points are listed from highest to lowest priority.

**Table 12 PALcode Trap Entry Points**

Entry Name	Offset <sub>16</sub>	Description
RESET	0000	Reset
IACCVIO	0080	Istream access violation or sign check error on PC
INTERRUPT	0100	Interrupt: hardware, software, and AST
ITBMISS	0180	Istream TBMISS
DTBMISS_SINGLE	0200	Dstream TBMISS
DTBMISS_DOUBLE	0280	Dstream TBMISS during virtual page table entry (PTE) fetch
UNALIGN	0300	Dstream unaligned reference
DFAULT	0380	Dstream fault or sign check error on virtual address
MCHK	0400	Uncorrected hardware error
OPCDEC	0480	Illegal opcode
ARITH	0500	Arithmetic exception
FEN	0580	Floating-point operation attempted with: <ul style="list-style-type: none"><li>• Floating-point instructions (LD, ST, and operates) disabled through FPE bit in the ICSR IPR</li><li>• Floating-point IEEE operation with data type other than S, T, or Q</li></ul>

## Required PALcode Function Codes

### 9.2 Required PALcode Function Codes

Table 13 lists opcodes required for all Alpha implementations. The notation used is *oo.fff*, where *oo* is the hexadecimal 6-bit opcode and *fff* is the hexadecimal 26-bit function code.

**Table 13 Required PALcode Function Codes**

Mnemonic	Type	Function Code
DRAINA	Privileged	00.0002
HALT	Privileged	00.0000
IMB	Unprivileged	00.0086

### 9.3 Opcodes Reserved for PALcode

Table 14 lists the opcodes reserved by the Alpha architecture for implementation-specific use. These opcodes are privileged and are only available in PALmode. Section 10.1.2 shows the opcodes reserved for PALcode.

**Table 14 Opcodes Reserved for PALcode**

Opcode	Architecture Mnemonic
1B	PAL1B
1F	PAL1F
1E	PAL1E
19	PAL19
1D	PAL1D