

Electrical Characteristics

11 Electrical Data

This section describes the electrical characteristics of the 21164 component and its interface pins. It is organized as follows:

- Electrical characteristics
- DC characteristics
- Clocking scheme
- AC characteristics
- Power supply considerations

11.1 Electrical Characteristics

Table 23 lists the maximum ratings for the 21164 and Table 24 lists the operating voltages.

Table 23 21164 Absolute Maximum Ratings

Characteristics	Ratings
Storage temperature	-55°C to 125°C (-67°F to 257°F)
Junction temperature	15°C to 90°C (59°F to 194°F)
Supply voltage	V_{ss} = -0.5 V, V_{ddi} = 2.5 V, V_{dd} = 3.3 V
Signal input or output applied	-0.5 V to 4.6 V
Typical V_{dd} worst case power @ V_{dd} = 3.3 V	
Frequency = 366 MHz	3.0 W
<i>For frequencies greater than 366 MHz, add 0.5 W for each 133 MHz.</i>	
Typical V_{ddi} worst case power @ V_{ddi} = 2.5 V	
Frequency = 366 MHz	27.5 W
<i>For frequencies greater than 366 MHz, add 5.0 W for each 66 MHz.</i>	

DC Characteristics

Caution: Stress beyond the absolute maximum rating can cause permanent damage to the 21164. Exposure to absolute maximum rating conditions for extended periods of time can affect the 21164 reliability.

Table 24 Operating Voltages

Nominal		Maximum		Minimum	
Vdd	Vddi	Vdd	Vddi	Vdd	Vddi
3.3 V	2.5 V	3.46 V	2.6 V	3.13 V	2.4 V

11.2 DC Characteristics

The 21164 is designed to run in a 3.3-V CMOS/TTL environment. The 21164 is tested and characterized in a CMOS environment.

11.2.1 Power Supply

The **Vss** pins are connected to 0.0 V, the **Vddi** pins are connected to 2.5 V \pm 0.1 V, and the **Vdd** pins are connected to 3.3 V \pm 5%.

11.2.2 Input Signal Pins

Nearly all input signals are ordinary CMOS inputs with standard TTL levels (see Table 25). (See Section 11.3.1 for a description of an exception—**osc_clk_in_h,1**.)

After power has been applied, input and bidirectional pins can be driven to a maximum dc voltage of **Vclamp** at a maximum current of **Iclamp** without harming the 21164. Refer to Table 25 for **Vclamp** and **Iclamp** values. Inputs greater than **Vclamp** will be clamped to **Vclamp** provided that the current does not exceed **Iclamp**. The 21164 may be damaged if the voltage exceeds **Vclamp** or the current exceeds **Iclamp**.

11.2.3 Output Signal Pins

Output pins are ordinary 3.3-V CMOS outputs. Although output signals are rail-to-rail, timing is specified to **Vdd**/2.

Note: The 21164 microprocessor chips do not have an onchip resistor for an output driver. Earlier versions of the 21164 have a 30- Ω (typical) onchip resistor for an output driver.

DC Characteristics

Bidirectional pins are either input or output pins, depending on control timing. When functioning as output pins, they are ordinary 3.3-V CMOS outputs.

Table 25 shows the CMOS dc input and output pins.

Table 25 CMOS DC Input/Output Characteristics

(Sheet 1 of 2)

Parameter		Requirements			
Symbol	Description	Min.	Max.	Units	Test Conditions
Vih	High-level input voltage	2.0	—	V	—
Vil	Low-level input voltage	—	0.8	V	—
Voh	High-level output voltage	2.4	—	V	Ioh = -6.0 mA
Vol	Low-level output voltage	—	0.4	V	Iol = 6.0 mA
Iil_pd	Input with pull-down leakage current	—	±50	µA	Vin = 0 V
Iih_pd	Input with pull-down current	—	200	µA	Vin = 2.4 V
Iil_pu	Input with pull-up current	—	-800	µA	Vin = 0.4 V
Iih_pu	Input with pull-up leakage current	—	±50	µA	Vin = Vdd V
Iozl_pd	Output with pull-down leakage current (tristate)	—	±100	µA	Vin = 0 V
Iozh_pd	Output with pull-down current (tristate)	—	300 ¹	µA	Vin = 2.4 V
Iozl_pu	Output with pull-up current (tristate)	—	-800	µA	Vin = 0.4 V
Iozh_pu	Output with pull-up leakage current (tristate)	—	±100	µA	Vin = Vdd V
Vclamp	Maximum clamping voltage	—	Vdd +1.0	V	Iclamp = 100 mA

DC Characteristics

Table 25 CMOS DC Input/Output Characteristics

(Sheet 2 of 2)

Parameter		Requirements			
Symbol	Description	Min.	Max.	Units	Test Conditions
I_{dd}	Peak power supply current for V_{dd} power supply	—	1.3 ²	A	V_{dd} = 3.465 V Frequency = 366 MHz <i>For frequencies greater than 366 MHz, add 0.4 A for each 133 MHz.</i>
I_{ddi}	Peak power supply current for V_{ddi} power supply	—	13.8	A	V_{ddi} = 2.6 V Frequency = 366 MHz <i>For frequencies greater than 366 MHz, add 2.4 A for each 66 MHz.</i>

¹ For chip speeds greater than 500 MHz, the maximum **I_{ozh_pd}** is 500 μA.

² This assumes sysclk ratio of 3 and worst case loading of output pins.

Most pins have low current pull-down devices to **V_{ss}**. However, two pins have a pull-up device to **V_{dd}**. The pull-downs (or pull-ups) are always enabled. This means that some current will flow from the 21164 (if the pin has a pull-up device) or into the 21164 (if the pin has a pull-down device) even when the pin is in the high-impedance state. All pins have pull-down devices, except for the pins in the following table:

Signal Name	Notes
tms_h	Has a pull-up device
tdi_h	Has a pull-up device
osc_clk_in_h	50 Ω to V_{term} (\approx V_{dd} /2) (See Figure 13)
osc_clk_in_l	50 Ω to V_{term} (\approx V_{dd} /2) (See Figure 13)
temp_sense	150 Ω to V_{ss}

Clocking Scheme

11.3 Clocking Scheme

Note: The preferred clock mode of the 21164 is 1×. This is a change from the earlier versions of the 21164, which had a preferred clock mode of 2×. Refer to Section 11.4.8 for more details.

The differential input clock signals **osc_clk_in_h,l** run at the internal frequency of the time base for the 21164. The output signal **cpu_clk_out_h** toggles with an unspecified propagation delay relative to the transitions on **osc_clk_in_h,l**.

System designers have a choice of two system clocking schemes to run the 21164 synchronous to the system:

1. The 21164 generates and drives out a system clock, **sys_clk_out1_h,l**. It runs synchronous to the internal clock at a selected ratio of the internal clock frequency. There is a small clock skew between the internal clock and **sys_clk_out1_h,l**.
2. The 21164 synchronizes to a system clock, **ref_clk_in_h**, supplied by the system. The **ref_clk_in_h** clock runs at a selected ratio of the 21164 internal clock frequency. The internal clock is synchronized to the reference clock by an onchip digital phase-locked loop (DPLL).

11.3.1 Input Clocks

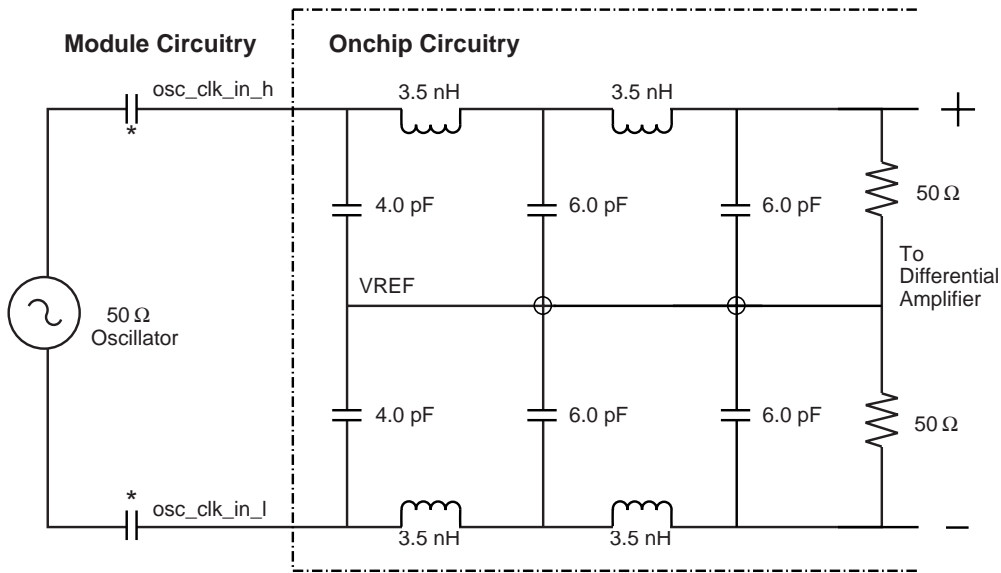
The differential input clocks **osc_clk_in_h,l** provide the time base for the chip when **dc_ok_h** is asserted. These pins are self-biasing, and must be capacitively coupled to the clock source on the module.

Note: It is not desirable to drive the **osc_clk_in_h,l** pins directly. This is a change from earlier versions of the 21164.

The terminations on these signals are designed to be compatible with system oscillators of arbitrary dc bias. The oscillator must have a duty cycle of 60%/40% or tighter. Figure 13 shows the input network and the schematic equivalent of **osc_clk_in_h,l** terminations.

Clocking Scheme

Figure 13 `osc_clk_in_h,l` Input Network and Terminations



Note:

* Coupling capacitors 47 pF to 220 pF

LJ-05357.A14

Ring Oscillator

When signal `dc_ok_h` is deasserted, the clock outputs follow the internal ring oscillator. The 21164 runs off the ring oscillator, just as it would when an external clock is applied. The frequency of the ring oscillator varies from chip to chip within a range of 10 MHz to 100 MHz. This corresponds to an internal CPU clock frequency range of 5 MHz to 50 MHz. The system clock divisor is forced to 8, and the `sys_clk_out2` delay is forced to 3.

Clock Sniffer

A special onchip circuit monitors the `osc_clk_in` pins and detects when input clocks are not present. When activated, this circuit switches the 21164 clock generator from the `osc_clk_in` pins to the internal ring oscillator. This happens independently of the state of the `dc_ok_h` pin. The `dc_ok_h` pin functions normally if clocks are present on the `osc_clk_in` pins.

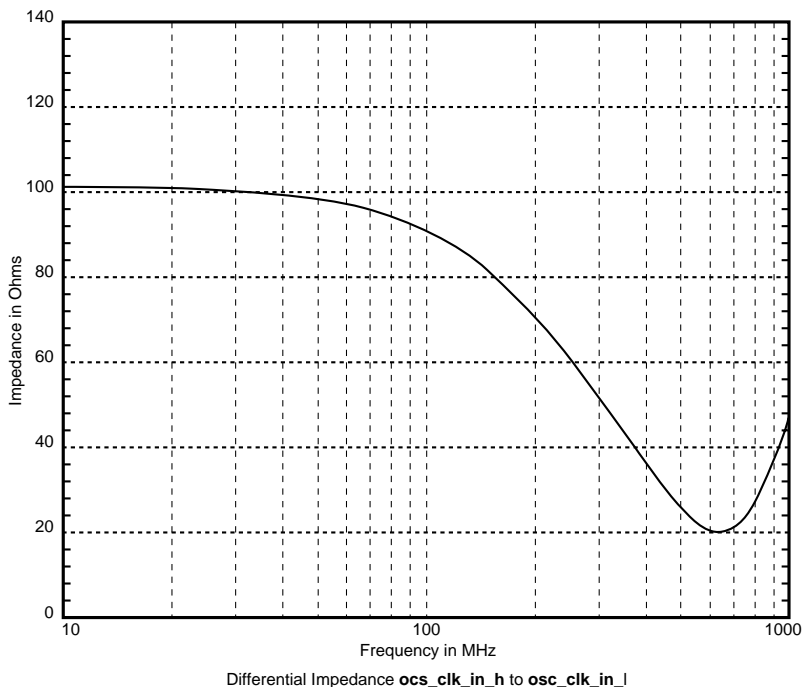
Clocking Scheme

11.3.2 Clock Termination and Impedance Levels

In Figure 13, the clock is designed to approximate a 50- Ω termination for the purpose of impedance matching for those systems that drive input clocks across long traces. The clock input pins appear as a 50- Ω series termination resistor connected to a high impedance voltage source. The voltage source produces a nominal voltage value of $V_{dd}/2$. The source has an impedance of between 130 Ω and 600 Ω . This voltage is called the self-bias voltage and sources current when the applied voltage at the clock input pins is less than the self-bias voltage. It sinks current when the applied voltage exceeds the self-bias voltage. This high impedance bias driver allows a clock source of arbitrary dc bias to be ac coupled to the 21164. The peak-to-peak amplitude of the clock source must be between 0.6 V and 3.0 V. Either a square-wave or a sinusoidal source may be used. Full-rail clocks may be driven by testers. In any case, the oscillator should be ac coupled to the **osc_clk_in_h,l** inputs by 47-pF through 220-pF capacitors.

Figure 14 shows a plot of the simulated impedance versus the clock input frequency. Figure 13 is a simplified circuit of the complex model used to create Figure 14.

Figure 14 Impedance vs Clock Input Frequency



LJ-04724.A15

AC Characteristics

11.3.3 AC Coupling

Using series coupling (blocking) capacitors renders the 21164 clock input pins insensitive to the oscillator's dc level. When connected this way, oscillators with any dc offset relative to V_{SS} can be used provided they can drive a signal into the **osc_clk_in_h,l** pins with a peak-to-peak level of at least 600 mV, but no greater than 3.0 V peak-to-peak.

The value of the coupling capacitor is not overly critical. However, it should be sufficiently low impedance at the clock frequency so that the oscillator's output signal (when measured at the **osc_clk_in_h,l** pins) is not attenuated below the 600-mV, peak-to-peak lower limit. For sine waves or oscillators producing nearly sinusoidal (pseudo square wave) outputs, 220 pF is recommended at 433 MHz. A high-quality dielectric such as NPO is required to avoid dielectric losses.

Table 26 shows the input clock specification.

Table 26 Input Clock Specification

Signal Parameter	Nominal Bin ¹	Unit
osc_clk_in_h,l symmetry	50 ± 10	%
osc_clk_in_h,l minimum voltage	0.6	V (peak-to-peak)
osc_clk_in_h,l Z input	50	Ω

¹ Minimum clock frequency = 50.0 MHz, Maximum clock frequency = 433 MHz = 1/Tcycle

11.4 AC Characteristics

This section describes the ac timing specifications for the 21164.

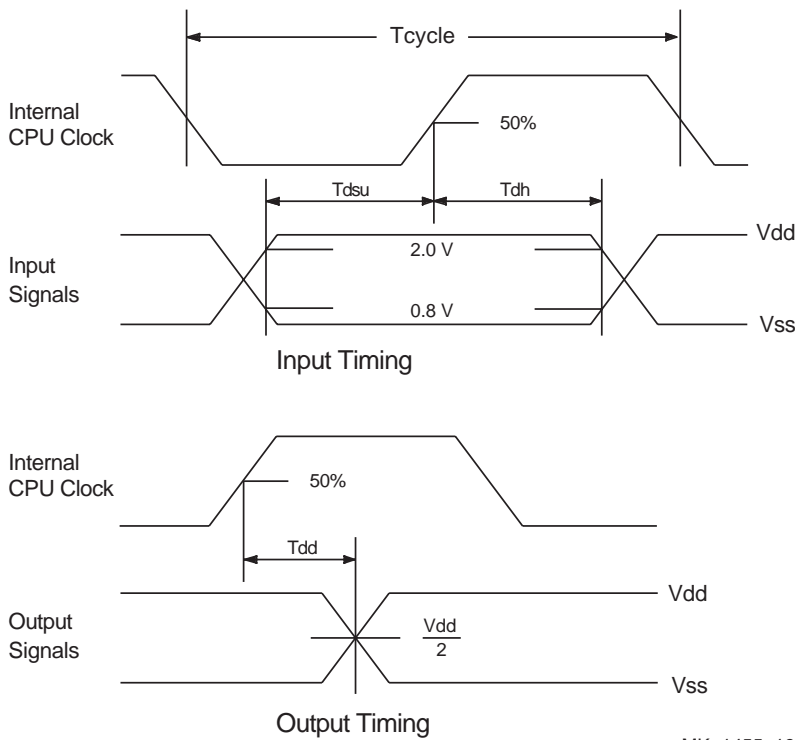
11.4.1 Test Configuration

All input timing is specified relative to the crossing of standard TTL input levels of 0.8 V and 2.0 V. Output timing is to the nominal CMOS switch point of $V_{DD}/2$ (see Figure 15).

Because the speed and complexity of microprocessors has increased substantially over the years, it is necessary to change the way they are tested. Traditional assumptions that all loads can be lumped into some accumulation of capacitance cannot be employed any more. Rather, the model of a transmission line with discrete loads is a much more realistic approach for current test technology.

AC Characteristics

Figure 15 Input/Output Pin Timing



MK-1455-19

Typically, printed circuit board (PCB) etch has a characteristic impedance of approximately 75Ω . This may vary from 60Ω to 90Ω with tolerances. If the line is driven in the electrical center, the load could be as low as 30Ω . Therefore, a characteristic impedance range of 30Ω to 90Ω could be experienced.

The 21164 output drivers are designed with typical printed circuit board applications in mind rather than trying to accommodate a 40-pF test load specification. As such, it “launches” a voltage step into a characteristic impedance, ranging from 30Ω to 90Ω .

There is no source termination resistor in the 21164 fabricated in 0.35- μm CMOS process technology. The source impedance of the driver is approximately $32 \Omega \pm 17$. The circuit is designed to deliver a TTL signal under worst case conditions. Under light load, high drive voltages, and fast process conditions there may be considerable overdrive. It may be necessary to install termination or clamping elements to the signal etches or loads.

AC Characteristics

11.4.2 Pin Timing

The following sections describe Bcache loop timing, sys_clk-based system timing, and reference clock-based system timing.

11.4.2.1 Backup Cache Loop Timing

The 21164 can be configured to support an optional offchip backup cache (Bcache). Private Bcache read or write (Scache victims) transactions initiated by the 21164 are independent of the system clocking scheme. Bcache loop timing must be an integer multiple of the 21164 cycle time.

Table 27 lists the Bcache loop timing.

Table 27 Bcache Loop Timing

Signal	Specification	Value		Name
		366 MHz – 500 MHz	Faster than 500 MHz	
data_h<127:0>	Input setup	1.2 ns	1.1 ns	Tdsu
data_h<127:0>	Input hold	0.0 ns	-0.1 ns	Tdh
data_h<127:0>	Output delay	Tdd + Tcycle + 0.4 ns¹	Tdd + Tcycle + 0.2 ns²	Tdod
data_h<127:0>	Output hold	Tmdd + Tcycle	Tmdd + Tcycle	Tdoh
index_h<25:4>, st_clk1_h, st_clk2_h³	Output delay	Tbedd + 0.4 ns, or Tbdd + 0.4 ns^{1,4}	Tbedd + 0.2 ns, or Tbdd + 0.2 ns^{2,4}	Tiod
index_h<25:4>, st_clk1_h, st_clk2_h³	Output hold time	Tmdd	Tmdd	Tioh

¹ The value 0.4 ns accounts for onchip driver and clock skew.

² The value 0.2 ns accounts for onchip driver and clock skew.

³ See 21164 change document for the positioning of **st_clk1_h** and **st_clk2_h** with respect to the Bcache index pins.

⁴ For big drive enabled or big drive disabled, respectively. See Table 29.

Outgoing Bcache index and data signals are driven off the internal clock edge and the incoming Bcache tag and data signals are latched on the same internal clock edge. Table 28 and Table 29 show the output driver characteristics for the normal driver and big driver respectively.

AC Characteristics

Additional drive for the following pins can be enabled by connecting **big_drv_en_h** to **Vdd**:

- **index_h<25:4>**
- **tag_ram_oe_h, tag_ram_we_h**
- **data_ram_oe_h, data_ram_we_h**
- **st_clk1_h, st_clk2_h**

If any of the previous pins are connected to lightly loaded lines (less than 40 pF) additional drive should not be enabled or the lines should be properly terminated to avoid transmission line ringing.

Table 28 Normal Output Driver Characteristics

Specification	40-pF Load	10-pF Load	Name
Maximum driver delay	2.7 ns	1.6 ns	Tdd
Minimum driver delay	1.0 ns	1.0 ns (0.6 ns ¹)	Tmdd

¹ For chip speeds greater than 500 MHz, the minimum delay is 0.6 ns.

Table 29 Big Output Driver Characteristics

Specification	60-pF Load	40-pF Load	10-pF Load	Name
Extra Drive Disabled				
Maximum driver delay	NA ¹	2.8 ns	1.7 ns	Tbddd
Minimum driver delay	NA ¹	1.0 ns	1.0 ns (0.6 ns ²)	Tmddd
Extra Drive Enabled				
Maximum driver delay	2.7 ns	2.2 ns	1.7 ns	Tbedd
Minimum driver delay	1.0 ns	1.0 ns	1.0 ns (0.6 ns ²)	Tmdd

¹ NA = Not applicable.

² For chip speeds greater than 500 MHz, the minimum delay is 0.6 ns.

Output pin timing is specified for lumped 40-pF and 10- pF loads for the normal driver and lumped 60-pF, 40-pF, and 10-pF loads for the big driver. In some cases, the circuit may have loads higher than 40 pF (60 pF for big driver). The 21164 can safely drive higher loads provided the average charging or discharging current from

AC Characteristics

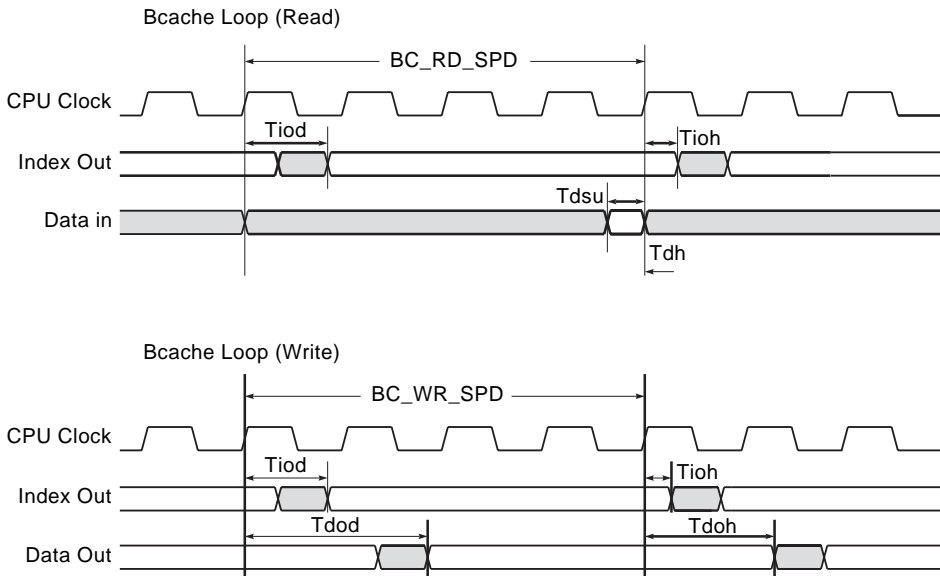
each pin is 11 mA or less for normal output drivers or 25 mA or less for big output drivers. The following equation can be used to determine the maximum capacitance that can be safely driven by each pin:

- For normal output drivers: C_{max} (in pF) = $5t$, where t is the waveform period (measured from rising to rising or falling to falling edge), in nanoseconds.
- For big output drivers: C_{max} (in pF) = $7t$, where t is the waveform period (measured from rising to rising or falling to falling edge), in nanoseconds.

For example, if the waveform appearing on a given normal I/O pin has a 15.0-ns period, it can safely drive up to and including 75 pF.

Figure 16 shows the Bcache read and write timing.

Figure 16 Bcache Timing



LJ-03409.A14

11.4.2.2 sys_clk-Based Systems

All timing is specified relative to the rising edge of the internal CPU clock.

Table 30 shows 21164 system clock **sys_clk_out1_h,l** output timing. Setup and hold times are specified independent of the relative capacitive loading of **sys_clk_out1_h,l**, **addr_h<39:4>**, **data_h<127:0>**, and **cmd_h<3:0>** signals. The **ref_clk_in_h** signal must be tied to **Vdd** for proper operation.

AC Characteristics

Table 30 21164 Reference Clock Input Timing

Signal	Specification	Value		Name
		366 MHz – 500 MHz	Faster than 500 MHz	
data_bus_req_h, data_h<127:0>, addr_h<39:4>	Input setup	1.2 ns	1.1 ns	Tdsu
data_bus_req_h, data_h<127:0>, addr_h<39:4>	Input hold	$0.5 \times T_{\text{cycle}}$	$0.5 \times T_{\text{cycle}}$	Troh
addr_h<39:4>	Output delay	$T_{\text{dd}} + 0.5 \times T_{\text{cycle}} + 0.9 \text{ ns}^1$	$T_{\text{dd}} + 0.5 \times T_{\text{cycle}} + 0.7 \text{ ns}^2$	Traod
addr_h<39:4>	Output hold time	Tmdd	Tmdd ³	Traoh
data_h<127:0>	Output delay	$T_{\text{dd}} + 1.5 + T_{\text{cycle}} + 0.9 \text{ ns}^1$	$T_{\text{dd}} + 1.5 + T_{\text{cycle}} + 0.7 \text{ ns}^2$	Trdod ⁴
data_h<127:0>	Output hold time	Tmdd + Tcycle	Tmdd ³ + Tcycle	Trdoh ⁴
Non-Pipe_Latch Mode				
addr_bus_req_h	Input setup	3.4 ns	3.4 ns	Tntrabrsu
addr_bus_req_h	Input hold	$0.5 \times T_{\text{cycle}}$	$0.5 \times T_{\text{cycle}}$	Tntrabrh
dack_h	Input setup	3.2 ns	3.2 ns	Tntracksu
cack_h	Input setup	3.4 ns	3.4 ns	Tntrcacksu
cack_h, dack_h	Input hold	$0.5 \times T_{\text{cycle}}$	$0.5 \times T_{\text{cycle}}$	Tntrackh
Pipe_Latch Mode ⁵				
addr_bus_req_h, cack_h, dack_h	Input setup	1.2 ns	1.1 ns	Ttracksu
addr_bus_req_h, cack_h, dack_h	Input hold	$0.5 \times T_{\text{cycle}}$	$0.5 \times T_{\text{cycle}}$	Ttrackh

¹ The value 0.9 ns accounts for onchip skews that include 0.4 ns for driver and clock skew, phase detector skews due to circuit delay (0.2 ns), and delay in **ref_clk_in_h** due to the package (0.3 ns).

² The value 0.7 ns accounts for onchip skews that include 0.2 ns for driver and clock skew, phase detector skews due to circuit delay (0.2 ns), and delay in **ref_clk_in_h** due to the package (0.3 ns).

³ For chip speeds greater than 500 MHz, **Tmdd** is 0.6 ns.

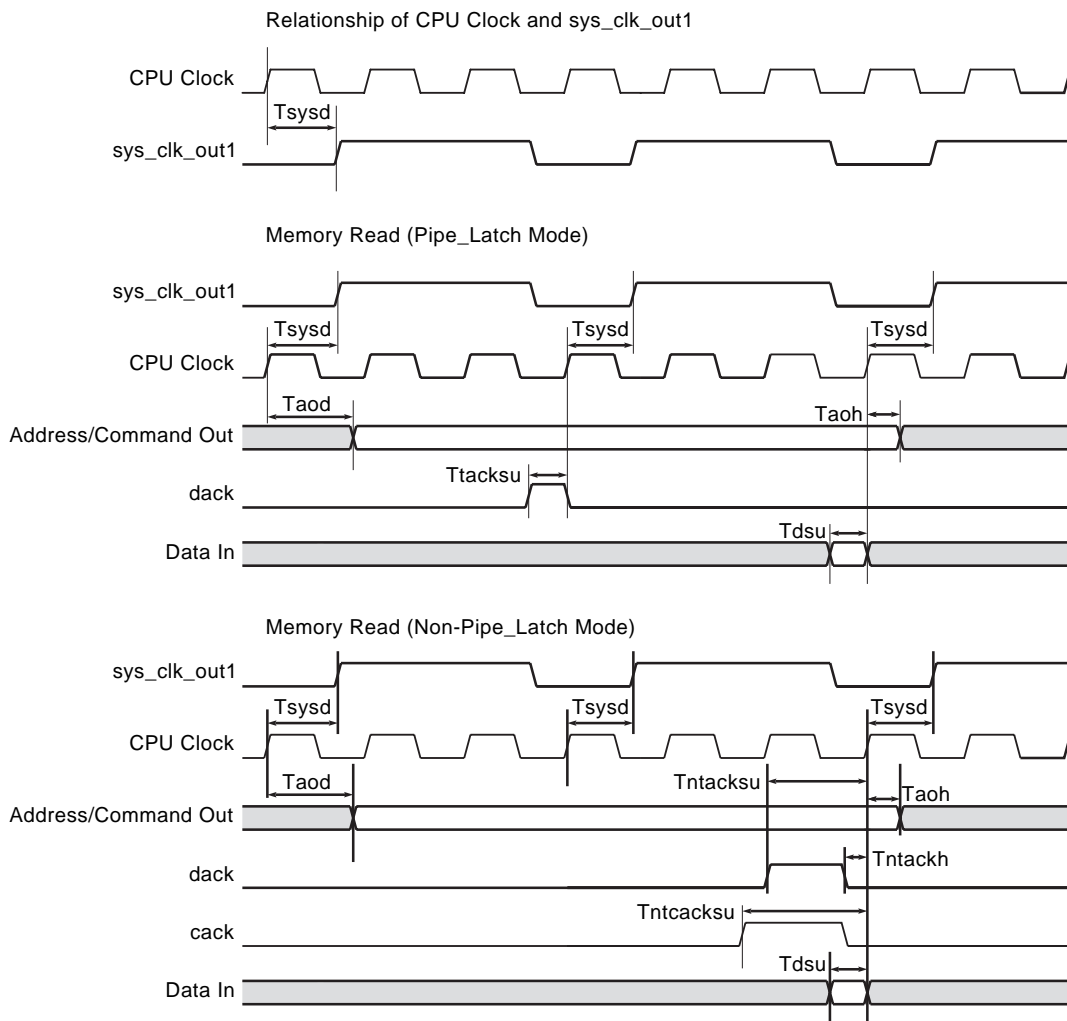
⁴ For all write transactions initiated by the 21164, data is driven one CPU cycle later.

⁵ In pipe_latch mode, control signals are piped onchip for one **sys_clk_out1_h,1** before usage.

AC Characteristics

Figure 17 shows `sys_clk` system timing.

Figure 17 `sys_clk` System Timing



LJ-03410.A14

11.4.2.3 Reference Clock-Based Systems

Systems that generate their own system clock expect the 21164 to synchronize its `sys_clk_out1_h,l` outputs to their system clock. The 21164 uses a digital phase-locked loop (DPLL) to synchronize its `sys_clk_out1` signals to the system clock that is applied to the `ref_clk_in_h` signal.

AC Characteristics

Table 31 shows all timing relative to the rising edge of **ref_clk_in_h**.

Table 31 21164 Reference Clock Input Timing

Signal	Specification	Value		Name
		366 MHz – 500 MHz	Faster than 500 MHz	
data_bus_req_h , data_h<127:0> , addr_h<39:4>	Input setup	1.2 ns	1.1 ns	Tdsu
data_bus_req_h , data_h<127:0> , addr_h<39:4>	Input hold	$0.5 \times \text{Tcycle}$	$0.5 \times \text{Tcycle}$	Troh
addr_h<39:4>	Output delay	$\text{Tdd} + 0.5 \times \text{Tcycle} + 0.9 \text{ ns}^1$	$\text{Tdd} + 0.5 \times \text{Tcycle} + 0.7 \text{ ns}^2$	Traod
addr_h<39:4>	Output hold time	Tmdd	Tmdd ³	Traoh
data_h<127:0>	Output delay	$\text{Tdd} + 1.5 + \text{Tcycle} + 0.9 \text{ ns}^1$	$\text{Tdd} + 1.5 + \text{Tcycle} + 0.7 \text{ ns}^2$	Trdod ⁴
data_h<127:0>	Output hold time	Tmdd + Tcycle	Tmdd ³ + Tcycle	Trdoh ⁴
Non-Pipe_Latch Mode				
addr_bus_req_h	Input setup	3.4 ns	3.4 ns	Tntrabrsu
addr_bus_req_h	Input hold	$0.5 \times \text{Tcycle}$	$0.5 \times \text{Tcycle}$	Tntrabrh
dack_h	Input setup	3.2 ns	3.2 ns	Tntracksu
cack_h	Input setup	3.4 ns	3.4 ns	Tntrcacksu
cack_h, dack_h	Input hold	$0.5 \times \text{Tcycle}$	$0.5 \times \text{Tcycle}$	Tntrackh
Pipe_Latch Mode ⁵				
addr_bus_req_h , cack_h, dack_h	Input setup	1.2 ns	1.1 ns	Ttracksu
addr_bus_req_h , cack_h, dack_h	Input hold	$0.5 \times \text{Tcycle}$	$0.5 \times \text{Tcycle}$	Ttrackh

¹ The value 0.9 ns accounts for onchip skews that include 0.4 ns for driver and clock skew, phase detector skews due to circuit delay (0.2 ns), and delay in **ref_clk_in_h** due to the package (0.3 ns).

² The value 0.7 ns accounts for onchip skews that include 0.2 ns for driver and clock skew, phase detector skews due to circuit delay (0.2 ns), and delay in **ref_clk_in_h** due to the package (0.3 ns).

³ For chip speeds greater than 500 MHz, **Tmdd** is 0.6 ns.

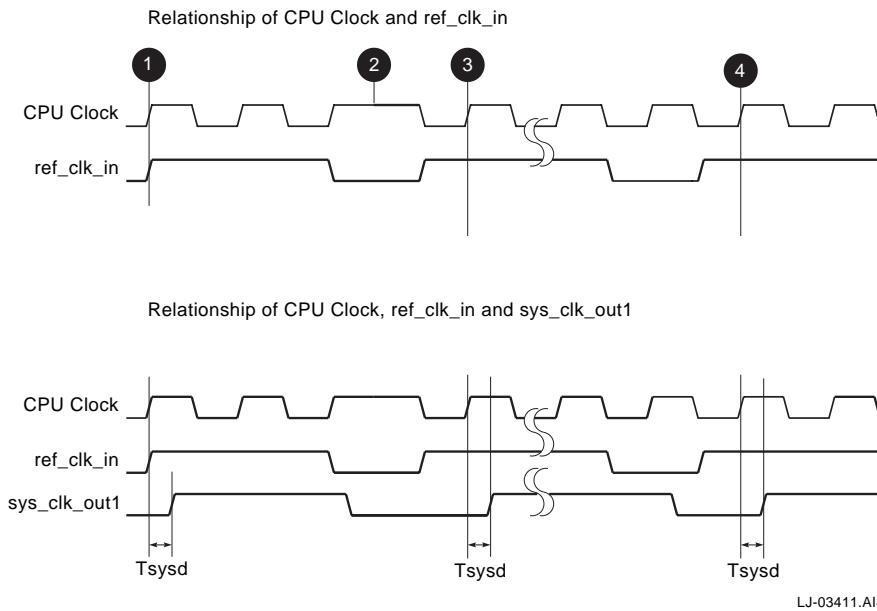
⁴ For all write transactions initiated by the 21164, data is driven one CPU cycle later.

⁵ In pipe_latch mode, control signals are piped onchip for one **sys_clk_out1_h,1** before usage.

11.4.3 Digital Phase-Locked Loop

Figure 18 and Table 32 describe the digital phase-locked loop (DPLL) stages of operation.

Figure 18 ref_clk System Timing



LJ-03411.A14

Table 32 describes the callouts shown in Figure 18.

Table 32 ref_clk System Timing Stages

Stage	Description
1	The internal CPU clock rising edge coincides with the rising edge of ref_clk_in_h .
2	The DPLL causes the internal CPU clock to stretch for one phase (1 cycle of osc_clk_in_h,l).
3	The stretch causes ref_clk_in_h to lead the internal CPU clock by one phase.
4	The CPU clock is always slightly faster than the external ref_clk_in_h and gains on ref_clk_in_h over time. Eventually the gain equals one phase and a new stretch phase follows.

AC Characteristics

Although systems that supply a **ref_clk_in_h** do not use **sys_clk_out1_h,l**, a relationship between the two signals exists, just as in the **sys_clk**-based systems, because the 21164 uses **sys_clk_out1_h,l** internally to determine timing during system transactions.

11.4.4 Timing—Additional Signals

This section lists timing for all other signals.

11.4.4.1 Asynchronous Input Signals

The following is a list of the asynchronous input signals:

clk_mode_h<2:0>	dc_ok_h	ref_clk_in_h	sys_reset_l²
oe_we_active_low_h	perf_mon_h¹	big_drv_en_h	irq_h<3:0>¹
mch_hlt_irq_h¹	pwr_fail_irq_h¹	sys_mch_chk_irq_h¹	

¹ These signals can also be used synchronously.

² Signal **sys_reset_l** may be deasserted synchronously.

AC Characteristics

11.4.4.2 Miscellaneous Signals

Table 33 and Table 34 list the timing for miscellaneous input-only and output-only signals. All timing is expressed in nanoseconds.

Table 33 Input Timing for sys_clk_out- or ref_clk_in-Based Systems

Signal	Specification	Value		Name	
		sys_clk_out	ref_clk_in	sys_clk_out	ref_clk_in
cfail_h, fill_h, fill_error_h, fill_id_h, fill_nocheck_h, idle_bc_h, shared_h, system_lock_flag_h	Input setup	1.2 ns (1.1 ns ¹)	1.2 ns (1.1 ns ¹)	Tdsu	Tdsu
irq_h<3:0>, mch_hlt_irq_h, pwr_fail_irq_h, sys_mch_chk_irq_h					
Testability pins: port_mode_h, srom_data_h, srom_present_l					
cfail_h, fill_h, fill_error_h, fill_id_h, fill_nocheck_h, idle_bc_h, shared_h, system_lock_flag_h	Input hold	0 ns (-0.1 ns ¹)	0.5 × Tcycle	Tdh	Troh
irq_h<3:0>, mch_hlt_irq_h, pwr_fail_irq_h, sys_mch_chk_irq_h					
sys_reset_l					
Testability pins: port_mode_h, srom_data_h, srom_present_l					

¹ For chip speeds greater than 500 MHz.

AC Characteristics

Table 34 Output Timing for sys_clk_out- or ref_clk_in-Based Systems (Sheet 1 of 2)

Signal	Specification	Clocking System Value		Clocking System Name	
		sys_clk_out	ref_clk_in	sys_clk_out	ref_clk_in
Unidirectional Signals					
addr_res_h, int4_valid_h, ¹ scache_set_h, srom_clk_h, srom_oe_l, victim_pending_h	Output delay	$T_{dd} + 0.4 \text{ ns}$ ($T_{dd} + 0.2 \text{ ns}^2$)	$T_{dd} +$ $0.5 \times T_{cycle} +$ 0.9 ns ($T_{dd} +$ $0.5 \times T_{cycle} +$ 0.7 ns^2)	Taod	Traod
addr_res_h, int4_valid_h, ¹ scache_set_h, srom_clk_h, srom_oe_l, victim_pending_h	Output hold	Tmdd	Tmdd ³	Taoh	Traoh
int4_valid_h ⁴	Output delay	$T_{dd} + T_{cycle} + 0.4 \text{ ns}$ ($T_{dd} + T_{cycle}$ $+ 0.2 \text{ ns}^2$)	$T_{dd} +$ $1.5 \times T_{cycle} +$ 0.9 ns ($T_{dd} +$ $1.5 \times T_{cycle} +$ 0.7 ns^2)	Tdod	Trdod
int4_valid_h ⁴	Output hold	Tmdd + Tcycle	Tmdd ³ + Tcycle	Tdoh	Trdoh
Bidirectional Signals					
Input mode:					
addr_cmd_par_h, cmd_h, data_check_h, ¹ tag_ctl_par_h, ⁵ tag_dirty_h, ⁵ tag_shared_h ⁵	Input setup	1.2 ns (1.1 ns ²)	1.2 ns (1.1 ns ²)	Tdsu	Tdsu
addr_cmd_par_h, cmd_h, data_check_h, ¹ tag_ctl_par_h, ⁵ tag_dirty_h, ⁵ tag_shared_h ⁵	Input hold	0 ns (-0.1 ns ²)	$0.5 \times T_{cycle}$	Tdh	Tsdadh

AC Characteristics

Table 34 Output Timing for sys_clk_out- or ref_clk_in-Based Systems (Sheet 2 of 2)

Signal	Specification	Clocking System Value		Clocking System Name	
		sys_clk_out	ref_clk_in	sys_clk_out	ref_clk_in
Output mode:					
addr_cmd_par_h , cmd_h , tag_ctl_par_h , ⁶ tag_dirty_h , ⁶ tag_shared_h , ⁶ tag_valid_h ⁶	Output delay	Tdd + 0.4 ns (Tdd + 0.2 ns ²)	Tdd + 0.5 × Tcycle + 0.9 ns (Tdd + 0.5 × Tcycle + 0.7 ns ²)	Taod	Traod
data_check_h ⁴	Output delay	Tdd + Tcycle + 0.4 ns (Tdd + Tcycle + 0.2 ns ²)	Tdd + 1.5 × Tcycle + 0.9 ns (Tdd + 1.5 × Tcycle + 0.7 ns ²)	Tdod	Trdod
addr_cmd_par_h , cmd_h , tag_ctl_par_h , ⁶ tag_dirty_h , ⁶ tag_shared_h , ⁶ tag_valid_h ⁶	Output hold	Tmdd	Tmdd ³	Taoh	Traoh
data_check_h ⁴	Output hold	Tmdd + Tcycle	Tmdd ³ + Tcycle	Tdoh	Trdoh

¹ Read transaction.

² For chip speeds greater than 500 MHz.

³ For chip speeds greater than 500 MHz, **Tmdd** is 0.6 ns.

⁴ Write transaction.

⁵ Fills from memory.

⁶ Only for write broadcasts and system transactions.

AC Characteristics

Signals in Table 35 are used to control Bcache data transfers. These signals are driven off the CPU clock. The choice of **sys_clk_out** or **ref_clk_in** has no impact on the timing of these signals.

Table 35 Bcache Control Signal Timing

Signal	Specification	Value		Name
		366 MHz–500 MHz	Faster than 500 MHz	
Input mode:				
tag_data_h, tag_data_par_h, tag_valid_h	Input setup	1.2 ns	1.1 ns	Tdsu
tag_data_h, tag_data_par_h, tag_valid_h	Input hold	0 ns	–0.1 ns	Tdh
Output mode:				
data_ram_oe_h, data_ram_we_h,¹ tag_ram_oe_h, tag_ram_we_h¹	Output delay	Tbedd + 0.4 ns ² or Tbddd + 0.4 ns ^{2,3}	Tbedd + 0.2 ns ² or Tbddd + 0.2 ns ^{3,4}	Taod
tag_data_h, tag_data_par_h, tag_valid_h	Output delay	Tdd + 0.4 ns ²	Tdd + 0.2 ns ⁴	Taod
data_ram_oe_h, data_ram_we_h,¹ tag_ram_oe_h, tag_ram_we_h¹	Output hold	Tmdd	Tmdd ⁵	Taoh
tag_data_h, tag_data_par_h, tag_valid_h	Output hold	Tmdd	Tmdd ⁵	Taoh

¹ Pulse width for this signal is controlled through the BC_CONFIG IPR.

² The value 0.4 ns accounts for onchip driver and clock skew.

³ For big drive enabled or big drive disabled, respectively. See Table 29.

⁴ The value 0.2 ns accounts for onchip driver and clock skew.

⁵ For chip speeds greater than 500 MHz, **Tmdd** is 0.6 ns.

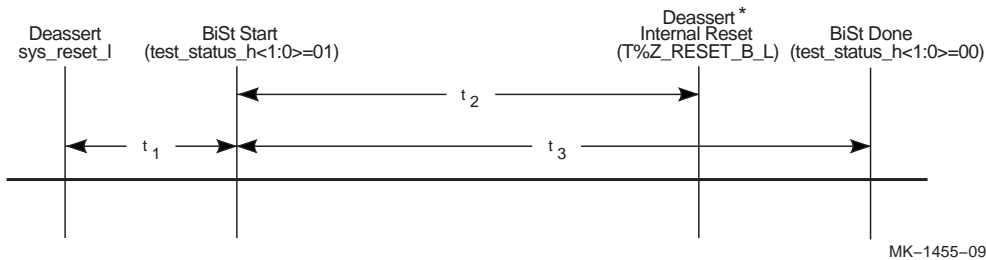
11.4.5 Timing of Test Features

Timing of 21164 testability features depends on the system clock rate and the test port's operating mode. This section provides timing information that may be needed for most common operations.

11.4.6 Icache BiSt Operation Timing

The Icache BiSt is invoked by deasserting the external reset signal **sys_reset_1**. Figure 19 shows the timing between various events relevant to BiSt operations.

Figure 19 BiSt Timing Event—Time Line



MK-1455-09

The timing for deassertion of internal reset (time t_2 , see asterisk) is valid only if an SROM is not present (indicated by keeping signal **srom_present_1** deasserted). If an SROM is present, the SROM load is performed once the BiSt completes. The internal reset signal T%Z_RESET_B_L is extended until the end of the SROM load (Section 11.4.7). In this case, the end of the time line shown in Figure 19 connects to the beginning of the time line shown in Figure 20.

Table 36 and Table 37 list timing shown in Figure 19 for some of the system clock ratios. Time t_1 is measured starting from the rising edge of sysclk following the deassertion of the **sys_reset_1** signal.

Table 36 BiSt Timing for Some System Clock Ratios, Port Mode=Normal (System Cycles)

Sysclk Ratio	System Cycles		
	t_1	t_2	t_3
3	8	22644 + 2½	22645
4	7	19721 + 2½	19722
15	7	13291 + 14½	13292

AC Characteristics

Table 37 BiSt Timing for Some System Clock Ratios, Port Mode=Normal (CPU Cycles)

Sysclk Ratio	CPU Cycles		
	t_1	t_2	t_3
3	24	67934½	67935
4	28	78886½	78888
15	105	199379½	199380

11.4.7 Automatic SROM Load Timing

The SROM load is triggered by the conclusion of BiSt if **srom_present_1** is asserted. The SROM load occurs at the internal cycle time of approximately 126 CPU cycles for **srom_clk_h**, but the behavior at the pins may shift slightly.

Timing events are shown in Figure 20 and are listed in Table 38 and Table 39.

Figure 20 SROM Load Timing Event—Time Line

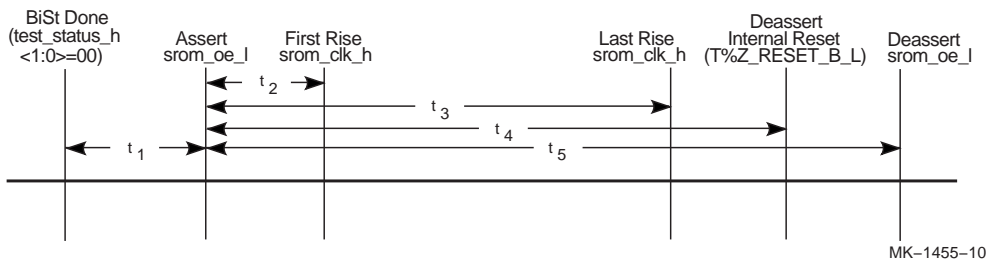


Table 38 SROM Load Timing for Some System Clock Ratios (System Cycles)

Sysclk Ratio	System Cycles ¹				
	t_1	t_2	t_3	t_4	t_5
3	4	22	4408090	4408216 + ½	4408217
4	3	48	3306099	3306193 + 2½	3306194
15	3	13	881627	881651 + 9½	881652

¹ Measured in sysclk cycles, where “+ n” refers to an additional n CPU cycles.

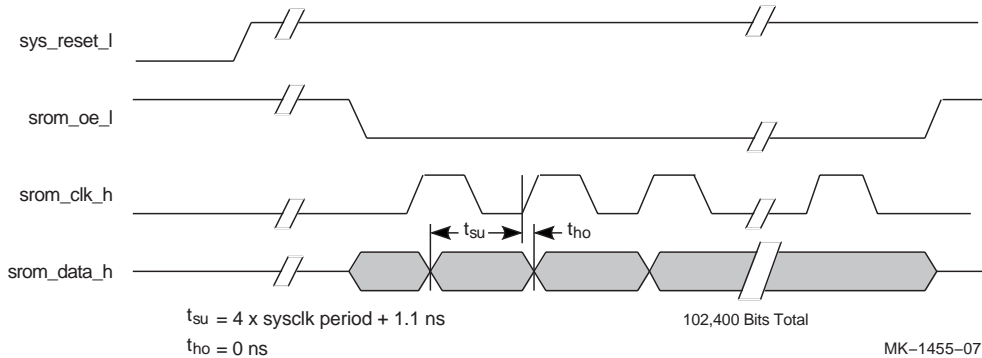
AC Characteristics

Table 39 SROM Load Timing for Some System Clock Ratios (CPU Cycles)

Sysclk Ratio	CPU Cycles				
	t_1	t_2	t_3	t_4	t_5
3	12	66	13224270	13224648½	13224651
4	12	192	13224396	13224774½	13224776
15	45	195	13224405	13224774½	13224780

Figure 21 is a timing diagram of an SROM load sequence.

Figure 21 Serial ROM Load Timing



The minimum `srom_clk_h` cycle = $(126 - \text{sysclk ratio}) \times (\text{CPU cycle time})$.

The maximum `srom_clk_h` to `srom_data_h` delay allowable (in order to meet the required setup time) = $[126 - (5 \times \text{sysclk ratio})] \times (\text{CPU cycle time})$.

11.4.8 Clock Test Modes

This section describes the 21164 clock test modes.

11.4.8.1 Normal (1× Clock) Mode

When `clk_mode_h<2:0>` = 101, the `osc_clk_in_h,l` frequency is not divided and a clock equalizing circuit (called a **symmetrator**) is enabled. The symmetrator equalizes the duty-cycle of the input clock for use onchip. The `osc_clk_in_h,l` signals must have a duty cycle of at least 60/40 for the symmetrator to work properly. This is the preferred clocking mode of the 21164.

AC Characteristics

11.4.8.2 2× Clock Mode

When `clk_mode_h<2:0> = 000`, the `osc_clk_in_h,l` frequency is divided by 2. The `osc_clk_in_h,l` signals must have a duty cycle of at least 60/40.

11.4.8.3 Chip Test Mode

To lower the maximum frequency that the chip manufacturing tester is required to supply, a divide-by-1 mode has been designed into the clock generator circuitry. When `clk_mode_h<2:0> = 001`, the clock frequency that is applied to the input clock signals `osc_clk_in_h,l` bypasses the clock divider and is sent to the chip clock driver. This allows the chip internal circuitry to be tested at full speed with a one-half frequency `osc_clk_in_h,l`.

Note: The clock symmetrator is not enabled in this mode.

11.4.8.4 Module Test Mode

When `clk_mode_h<2:0> = 010`, the clock frequency that is applied to the input clock signals `osc_clk_in_h,l` is divided by 4 and is sent to the chip clock driver. The digital phase-locked loop (DPLL) continues to keep the onchip `sys_clk_out1_h,l` locked to `ref_clk_in_h` within the normal limits if a `ref_clk_in_h` signal is applied (0 ns to 1 `osc_clk_in_h,l` cycle after `ref_clk_in_h`).

11.4.8.5 Clock Test Reset Mode

When `clk_mode_h<2:0> = 011`, the `sys_clk_out` generator circuit is forced to reset to a known state. This allows the chip manufacturing tester to synchronize the chip to the tester cycle. Table 40 lists the clock test modes.

Table 40 Clock Test Modes

(Sheet 1 of 2)

Mode	clk_mode_h		
	<2>	<1>	<0>
Normal (1×) clock mode	1	0	1
2× clock mode	0	0	0
Chip test	0	0	1
Module test	0	1	0

Power Supply Considerations

Table 40 Clock Test Modes

(Sheet 2 of 2)

Mode	clk_mode_h		
	<2>	<1>	<0>
Clock reset	0	1	1
Not valid	1	0	0
Not valid	1	1	x

11.4.9 IEEE 1149.1 (JTAG) Performance

Table 41 lists the standard mandated performance specifications for the IEEE 1149.1 circuits.

Table 41 IEEE 1149.1 Circuit Performance Specifications

Item	Specification
trst_l is asynchronous. Minimum pulse width.	4 ns
trst_l setup time for deassertion before a transition on tck_h .	4 ns
Maximum acceptable tck_h clock frequency.	16.6 MHz
tdi_h/tms_h setup time (referenced to tck_h rising edge).	4 ns
tdi_h/tms_h hold time (referenced to tck_h rising edge).	4 ns
Maximum propagation delay at pin tdo_h (referenced to tck_h falling edge).	14 ns
Maximum propagation delay at system output pins (referenced to tck_h falling edge).	20 ns

11.5 Power Supply Considerations

For correct operation of the 21164, all of the **Vss** pins must be connected to ground, all of the **Vdd** pins must be connected to a 3.3-V $\pm 5\%$ power source, and all of the **Vddi** pins must be connected to a 2.5-V ± 0.1 V power source. This source voltage should be guaranteed (even under transient conditions) at the 21164 pins, and not just at the PCB edge.

Plus 5 V is not used in the 21164. The voltage difference between the **Vdd** pins and **Vss** pins must never be greater than 3.46 V, and the voltage difference between the **Vddi** pins and **Vss** pins must never be greater than 2.6 V. If the differentials exceed these limits, the 21164 chip will be damaged.

Power Supply Considerations

11.5.1 Decoupling

The effectiveness of decoupling capacitors depends on the amount of inductance placed in series with them. The inductance depends both on the capacitor style (construction) and on the module design. In general, the use of small, high-frequency capacitors placed close to the chip package's power and ground pins with very short module etch will give best results. Depending on the user's power supply and power supply distribution system, bulk decoupling may also be required on the module.

The 21164 requires two sets of decoupling capacitors: one for **Vdd** and one for **Vddi**.

11.5.1.1 Vdd Decoupling

The amount of decoupling capacitance connected between **Vdd** and **Vss** should be roughly equal to 10 times the amount of capacitive load that the 21164 is required to drive at any one time. This should guarantee a voltage drop of no more than 10% on **Vdd** during heavy drive conditions.

Use capacitors that are as physically small as possible. Connect the capacitors directly to the 21164 **Vdd** and **Vss** pins by short surface etch (0.64 cm [0.25 in] or less). The small capacitors generally have better electrical characteristics than the larger units and will more readily fit close to the IPGA pin field.

When designing the placement of decoupling capacitors, **Vdd** decoupling capacitors should be favored over **Vddi** decoupling capacitors (that is, **Vdd** capacitors should be placed closer to the 21164 than the **Vddi** capacitors).

11.5.1.2 Vddi Decoupling

Each individual case must be separately analyzed, but generally designers should plan to use at least 4 μF of capacitance connected between **Vddi** and **Vss**. Typically, 30 to 40 small, high-frequency 0.1- μF capacitors are placed near the chip's **Vddi** and **Vss** pins. Actually placing the capacitors in the pin field is the best approach. Several tens of μF of bulk decoupling (comprised of tantalum and ceramic capacitors) should be positioned near the 21164 chip.

Use capacitors that are as physically small as possible. Connect the capacitors directly to the 21164 **Vddi** and **Vss** pins by short surface etch (0.64 cm [0.25 in] or less). The small capacitors generally have better electrical characteristics than the larger units, and will more readily fit close to the IPGA pin field.

Power Supply Considerations

11.5.2 Power Supply Sequencing

When applying or removing power to the 21164, **Vdd** (the 3.3-V supply voltage) must be no less than **Vddi** (the 2.2-V supply voltage).

The following rules must be followed when either applying or removing the supply voltages:

1. **Vdd** must always be at the same or a higher voltage than **Vddi** during normal operation
2. The *signal voltage* must not exceed **Vclamp**
3. The *signal voltage* must not be more than 2.4 V higher than **Vddi**

Rule 1 means that either **Vdd** and **Vddi** can be brought up and down in unison or **Vddi** can be applied after and removed before **Vdd**.

Rule 2 means that the signal voltage must not be allowed to exceed **Vclamp** during the application or removal of power. Refer to Table 25 for the value of **Vclamp**. Note that it is acceptable for the signal voltage either to be held at zero or to follow **Vdd** during the application or removal of power.

Rule 3 means that, if the signal voltage follows **Vdd**, the signal voltage must never be greater than 2.4 V above the value of **Vddi**. This applies equally during the application or the removal of power.

Note that if the signal voltage is held at 0 V during power-up reset (that is, the ASICs and SRAMs are set to drive 0 V during reset), **Vdd** and **Vddi** can be brought up together. In a similar manner, the power-down situation can be managed if the signal voltages are forced to 0 V when the loss of **Vddi** is detected.

During power-up, **Vddi** can momentarily exceed the maximum steady-state value under the following conditions:

- The transient voltage is 200 mV or less.
- The transient period lasts for 200 μ s or less.

The transient voltage is defined as the voltage that rises above the maximum-allowed steady-state value. The transient period is defined as the time beginning when the transient voltage exceeds the steady-state value and ending when it falls back to it.

There is no derating for shorter transient periods or lower transient voltages (for example, a 400-mV transient voltage lasting for 100 μ s is not acceptable).

Power Supply Considerations

All input and bidirectional signals are diode-clamped to **V_{dd}** and **V_{ss}**. A current greater than **I_{clamp}** on an individual pin could damage the 21164. Designers must take care that currents greater than **I_{clamp}** will not be achieved during power-supply sequencing. While currents less than **I_{clamp}** will not damage the 21164, other source drivers connected to the 21164 could be damaged by the clamp. Designers must verify that the source drivers will not be damaged by currents up to **I_{clamp}**.